VERTICAL POWER MOSFET STRUCTURE HAVING REDUCED CELL AREA

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power semiconductor device, and more specifically to a vertical power MOSFET (metal-oxide-semiconductor field effect transistor) and a method for manufacturing the same.

2. Description of Related Art

In "IEEE Transactions on Electron Devices", Vol. ED-32, No., January 1985, pages 2-6, UEDA et al has proposed a vertical power MOSFET structure with an extremely reduced on-resistance, which is called a rectangular-grooved MOSFET.

This vertical power MOSFET includes a silicon substrate, a drain layer formed on the silicon substrate, a base layer formed on the drain layer, and a source layer formed on the base layer. A plurality of rectangular-grooves are formed to extent downward from a surface of the source layer through the base layer so as to reach the drain layer. An inner surface of the grooves thus formed is coated with a gate insulator, and a gate electrode formed of a polysilicon is deposited on the gate insulator. In addition, an interlayer insulator is covered on each gate electrode and to fill into each of the grooves. On the other hand, between each pair of adjacent grooves, a contact hole for formation of a back gate is formed to extend downward from a surface of the source layer to reach the base layer, and a metal electrode is filled into the contact hole. An aluminium source electrode is deposited on the interlayer insulator and the metal electrode filled into the contact hole, so that the source electrode is in electrical contact with the source layer and the base layer.

For example, in the case of the rectangular-grooved vertical power MOSFET having a breakdown voltage of 60 V, an N^+ silicon substrate doped with antimony at a concentration of $2\times10^{18}/cm^3$ is prepared, and a layer having a thickness of about 20 μm and doped with phosphorus so as to have a specific resistance of 1Ω cm is epitaxially grown on the substrate. This phosphorus doped layer forms an N-type drain layer. Thereafter, a P-type base layer is formed on the surface of the drain layer by ion-implantation and heat-diffusion, and an N-type source layer is formed on the surface of the base layer by ion-implantation and heat-diffusion. Then, a plurality of trench grooves are formed by a photoresist process and an anisotropic etching, and an oxide film having a thickness of about 100 nm is formed on a surface of the substrate including an inner surface of the trench groove formed. The oxide film is selectively removed by a photoresist process so that only a gate oxide remains.

Thereafter, a polysilicon film having a thickness of about 600 nm is deposited by means of a LPCVD (low pressure chemical vapor deposition) process, and phosphorus is diffused in the deposited polysilicon film so that the polysilicon film has a sheet resistance of about 11$\Omega/\square$. Further, the doped polysilicon film is selectively removed and patterned by a photoresist process so as to form the gate electrode composed of the polysilicon film. Then, an interlayer insulator film is deposited by a CVD process, and contact holes for back gates are formed by the photoresist process and anisotropic etching. A tungsten is grown within the contact holes by means of a selective CVD process so as to substantially completely fill the contact holes. Finally, an aluminum source electrode is formed by a Sputtering so that the deposited source electrode is in electrical contact with the tungsten electrode filled in the contact holes.

In the above mentioned conventional process, in order to form the contact holes for the back gate by means of the photoresist process, it is necessary to ensure a margin for alignment and a side or lateral etching. In the ease of the vertical power MOSFET having a breakdown voltage of 60 V, a distance between the contact hole and the gate electrode was required to have not less than 2.5 μm. In addition, the tungsten electrode was necessary to have a lateral width of not less than 5 μm.

The above mentioned problems were similar in the case of an ordinary vertical power MOSFET in which no rectangular-groove for the gate electrode is formed and the gate electrode is formed on a planar upper surface of a substrate through a gate oxide. In the ordinary vertical power MOSFET, in addition, when an oxide film coveting a side surface of the gate electrode is formed, it was also necessary to ensure a margin for alignment and a side or lateral etching.

Accordingly, in the prior art vertical power MOSFETs, a microminiaturization of the back gate part is limited by the margin for alignment in the photolithography and a side or lateral etching.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a vertical power MOSFET and a method for manufacturing the same, which have overcome the above mentioned defect of the conventional ones.

Another object of the present invention is to provide a vertical power MOSFET having a reduced size of back gate part, and a method for manufacturing the same.

The above and other objects of the present invention are achieved in accordance with the present invention by a vertical power field effect transistor comprising a drain region of a first conductivity type semiconductor, a base region of a second conductivity type semiconductor and formed in contact with the drain region, a source region of the first conductivity type semiconductor and formed in contact with the base region, a gate insulator film formed to cover the source region, the base region and the drain region and to extend in such a manner as to locate the base region between the source region and the drain region, a gate electrode formed on the gate insulator film, a side insulator film formed on the source region so as to cover a side surface of the gate electrode and the gate insulator film, a groove formed in alignment with a surface of the side insulator film so as to extend downward from a semiconductor surface and to reach the base region, and a metal film filled in the groove.

According to another aspect of the present invention, there is provided a method for manufacturing the above mentioned vertical power field effect transistor, comprising the steps of forming an interlayer insulator film on the gate electrode, depositing an insulator film on a whole surface, anisotropically etching the deposited insulator film so that the deposited insulator film remains only on each side surface of the gate electrode so as to form a side insulator film, etching the source region using the side insulator film as a mask, so that a